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On the Analysis of Reversible Booth's Multiplier

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Abstract: Reversible logic attains the attraction of researchers in the last decade mainly due to low-cost, less area and low power dissipation. Designers' endeavors are thus continuing in creating complete reversible circuits consisting of reversible gates. This paper presents a design methodology for the realization of Booth's multiplier in reversible mode. Booth's multiplier is considered as one of the fastest multipliers in literature and we have shown an efficient design methodology in reversible paradigm. The proposed architecture is capable of performing both signed and unsigned multiplication of two operands without having any feedbacks, whereas existing multipliers in reversible mode consider loop which is strictly prohibited in reversible logic design. Theoretical underpinnings, established for the proposed design, show that the proposed circuit is very efficient from reversible circuit design point of view.

1INTRODUCTION

The field of reversible logic is achieving a growing interest by its possibility in quantum computing, low-power CMOS, nanotechnology, and optical computing. It is now widely accepted that the CMOS technology implementing irreversible logic will hit a scaling limit, and thus the increased power dissipation is a major limiting factor principle states that, logic computations that are not reversible generate heat for every bits of information that is lost. According to Frank computers based on reversible logic operations can reuse a fraction of signal energy that theoretically can approach arbitrarily near 100%. An n-input n-output function (gate) is called reversible if and only if it maps each input instance to a unique output instance. The only possible structure for a reversible network is the cascade of reversible gates. In practice, not all of the n! possible reversible

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functions can be realized as a single reversible gate. Several reversible gates have been proposed in literature so far, where the synthesis of reversible circuits differs significantly from synthesis in traditional irreversible mcircuits. Two restrictions are added for reversible networks, namely fan-outs and back-feeds. The aim of the paper is to design a Booth's multiplier in reversible mode which is capable of working with both signed and unsigned numbers. The reversible multiplier designed works for unsigned numbers only, while the recently developed one is based on booth recoding. On the other hand, the proposed design is dedicated to eliminate these limitations and prove its supremacy thereby. This design also establishes its efficiency by assimilating all the good features of reversible circuits that are characterized by number of garbage outputs and number of gates. Rest of the paper is organized as follows: After illustrating the preliminaries of reversible logic gates, we have presented the input-output vectors of popular reversible gates along with their quantum costs. concentrates on the main logic synthesis of the proposed reversible multiplier with the detailed description of each designed blocks. The theoretical underpinnings and the evaluation of the proposed Booth's multiplier are shown. We conclude discussing the main contribution and the future work.

2 LITERATURE REVIEW

Definition 1: A Reversible Gate is a k-input, k-output circuit that produces a unique output pattern for each possible input pattern. Reversible Gates are circuits in which the number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs, i.e., it can generate unique output vector from each input vector and vice versa. A reversible circuit must incorporate reversible gates in it and the number of gates used in a design is always a good complexity measure for the circuit. It is always desirable to realize a circuit with minimum number of gates.

Definition 2: Unwanted or unused output of a reversible gate (or circuit) is known as Garbage Output. More formally, the outputs which are needed only to maintain reversibility are called garbage outputs.

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While performing EXOR operation with a Feynman gate the second output should be called as garbage.

Definition 3: The delay of a logic circuit is the maximum number of gates in a path from any input line output line. The delay of the circuit is obviously 1 as it is the only gate in any path from input to output.

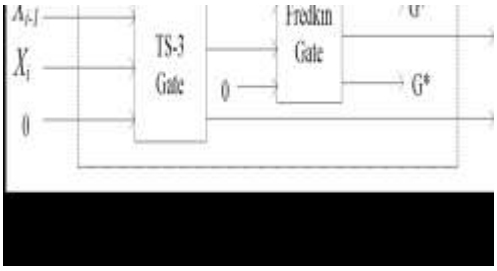
Definition 4: The quantum cost (QC) of gate costs nothing since it can be always included to arbitrary gate that precedes or follows it. Thus, in first approximation, every permutation of quantum gate will be built quantum primitives and its cost is calculated as the total sum that is used in the circuit. Now we define some popular reversible gates. I with their corresponding input-output vectors and quantum cost.

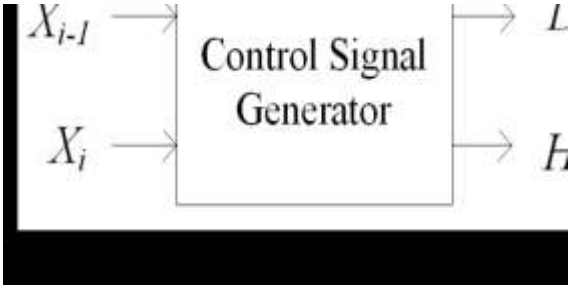
3 PROPOSED REVERSIBLE BOOTH'S MULTIPLIER

In this section, in a gradual approach we show the design of reversible array multiplier using Booth's algorithm. Implementing the Booth's method by a combinatorial array first requires a reversible multi-function cell capable of addition, subtraction and no operation (or skip), which we call as *B* cell according to the convention. The various function of *B* cell is selected by a couple of control lines named as *H* and *D*. The ontrol signal is generated by another control cell which is named as *C* cell.

Design of C Cell:

The *C* cell is the basic unit of control circuitry of the original array multiplier. The input of this cell implies two adjacent bits of the multiplier operand. The cell generates the required control signal named according to the original multiplier algorithm. Shows the input and output line of *C* cell.





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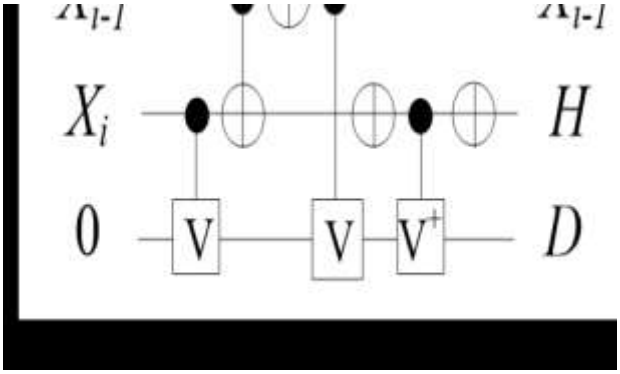


Design of B cell

The B cell is a multi-function cell, where various functions include addition, subtraction, and no-operation. These functions are defined by the following logic **equations:**

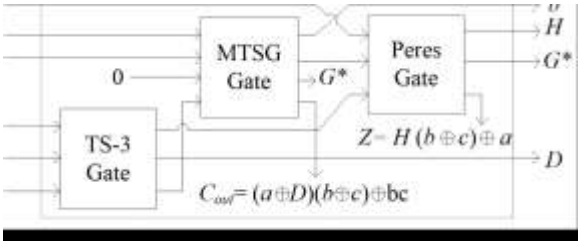
Z = a ⊕ bH ⊕ cH = a ⊕ (b ⊕ c) H Cout = (a ⊕ D) (b ⊕ c) ⊕ bc Here Z is the result of addition or subtraction and Cout indicates the carry output. The cell operates on three operands a, b, c where a is the propagated result from a previous B cell, b is a multiplicand bit and c is the carry-in bit. H and Dare the control signal generated by the corresponding C cell. When HD=10, these equations reduce to the usual full adder **equations:**

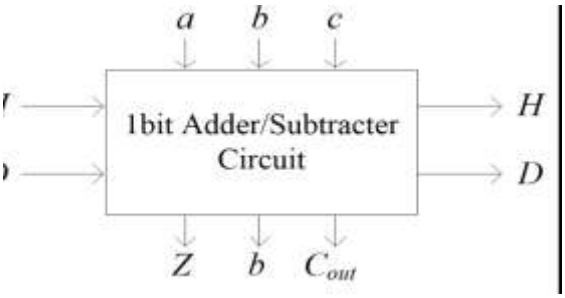
Sum = a ⊕ b ⊕ c Cout = ab ⊕ c (a ⊕ b)

On the contrary, when HD=11, the equations are converted to the corresponding full-subtracted equations:

Sum = a ⊕ b ⊕ c Cout = ab + ac + bc

When H=0, Z becomes a and the carry lines play no role in the final result. Table II summarizes the function of this cell.





Construction of n×n Reversible Twos Complement Array Multiplier

In this section, an n × n reversible Booth's multiplier is realized by the proposed B cell and C cell. The architecture of the n×n array multiplier, takes the form of a trapezium. All the C cells at the right together comprise the control circuitry. If X = Xn,Xn−1,Xn−2 . . . X0 and Y = Yn, Yn−1, Yn−2 . . . Y0 denote the multiplier and multiplicand,

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respectively then the multiplier bits are fed to the C cells, and a implicit zero is added with the multiplier bits. There are total n rows and each row contains a C cell, hence the total n number of C cells are required in the design. The top most row of this two dimensional architecture contains (2n-1) B cells. The second row consists of (2n-2) B cells. Continuing in this fashion the bottom line only contains n number of B cell. All the multiplicand bits are fed to the upper layer B cells (through the input line indicated by 'b' . The 'b' inputs of the left side of (n-1) B cells are set to the sign extended Y for addition and subtraction. The a inputs (indicates the result of sum or subtract from the corresponding upper layer cell) of the upper layer B cells and the carry inputs of the rightmost B cells are set to zero.

Multiplication Example by a 4×4 Reversible Booth's Multiplier

This section illustrates an example of multiplication by the proposed design. It shows the value of each input and output line for every single cell for the particular example. Assume that the two operands are −3 and 5, and so the result should be −15. Obviously the negative input that is the multiplicand will be in twos complement form. Hence, multiplicand Y =1101 (in twos complement form), multiplier X= 0101 (5), an implicit 0 is added, which becomes, X=01010 and they are fed into the C cells in the following manner.

01: HD=10 implies add.

10: HD=01 implies subtract.

01: HD=10 implies add.

10: HD=01 implies subtract.

Thus, the 4×4 circuit generates 1110001, which is -15 in two's complement.

4. EVALUATION OF THE ROPOSED DESIGN

In this section necessary theorems are given to evaluate the proposed design. All the theorems provide lower bounds for number of gates, garbage outputs, circuit delay and

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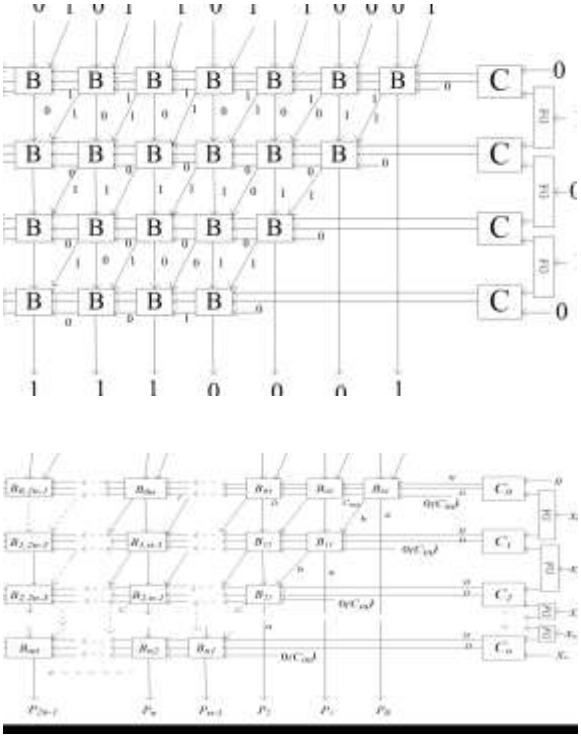
quantum cost.



Theorem 1: Let *NGT* be the number of gates required to realize an $n \times n$ Reversible Multiplier where n is the number of bits, then $NGT \geq 9\ 2\ n2 + 1$ (5)

Proof: An $n \times n$ Reversible Multiplier requires 3/2 $n(n\text{-}1)B$ cells and each *B* cell contains 3 reversible gates. Moreover, n *LB* cells (B cells in left most side) are required along with the *B* cell each of which contains 2 reversible gates. To perform the control operation n *C* cells are required, where each of them consists of 2 gates. Furthermore, $(n/2+1)$ FGs are required to perform the copy operation. As *NGT* is the total number of gates to realize the $n \times n$ Multiplier, according to the above definition:

$NGT \geq 3\ 2\ n\ (n - 1)3 + 2n + 2n + n\ 2 + 1$

$NGT \geq 9\ 2\ n2 + 1$

Similarly, we propose the following theorems that can be proved in the similar way.

Theorem 2: Let n be the number of bits in the Reversible Multiplier and *NGB* denotes the number of garbage outputs, then

$NGB \geq n\ (4n + 1) - 1$

Proof: Each *B* cell generates 2 garbage output and an $n \times n$ Reversible Multiplier requires 3/2 $n(n-1)$ *B* cells. The *LB* cell, comprises the last column of the reversible multiplier do not need to generate the carry equation as well as to propagate the control signal. Realization of a *LB* cell requires no less than 3 garbage output. Further, each *C* cell generates 2 garbage output and Total $2n$ number of garbage is added for n *C* cells. oreover, $(n\text{-}1)$ *B* cells of the last row generates extra $(n\text{-}1)$ garbage that is due to the propagation of prime input b. As *NGB* is considered as the minimum number of gates to realize the reversible multiplier, hence

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$NGB \geq 3\ 2\ n(n-1)2 + 3n + 2n + (n-1)$

$NGB \geq n(4n+1) - 1$

Theorem 3: Let $P\_\_$, $\_$ and Pare the delay of *B*, *LB* and *C* cell respectively in the $n \times n$ reversible multiplier. Let, *DF* be the delay of a FG and *DRM* denotes the total delay of the reversible multiplier, then$DRM \geq (2n-2)P__ + nP_ + P + DF$

Proof: The longest path from input to output of the $n \times n$ Reversible Multiplier contains 2(*n*-1) *B* cells which incurs a delay of 2(*n*-1) *P*__. In addition, the path also contains *n LB* cell, one *C* cell and a FG along with the *B* cell. Hence, considering *DRM* as the total delay, $DRM \geq (2n-2)\ P\_\_ + Np\_ + P + DF$

Theorem 4: Let QC (RM) be the total quantum cost to realize an n × n reversible multiplier where n is the number of bits, then QC(RM) ≥ 18n2 + 13 n 2 + 1

Proof: Each B cell tenders a quantum cost of 12 (QC(TS- 3)+QC(MTSG) + QC(PG)= 2+6+4). An n × n reversible multiplier requires n/2(3n − 5) such B cells. The B cell of the column before the last one uses FG instead of TS-3 since it does not need to feed control signal D to the last level of LB cell. Thus, each B cell of this specific column incurs a quantum cost of 11. Moreover the quantum cost of each individual LB cell is 5 (QC (FG)+ QC(PG)= 1+4). Beside this, the n number of C cells contribute 7n to the quantum cost and the remaining (n/2+1) FGs are responsible for a QC of (n/2+1). As QC (RM) is the total quantum cost to realize the n × n multiplier, according to the aforementioned definition:

QC (RM) ≥ n 2 (3n − 5)12 + 11n + 5n + 7n + N 2 + 1 ≥ ≥ 18n2 + 13 n 2 + 1.

We also evaluate the 4×4 version of the proposed Booth's multiplier with the two existing designs. To compute the necessary parameters for a 4×4 array multiplier the instance of the generalized equations are taken and the calculation is carried out by putting the value of n = 4. Existing method of Bhardaj and Deshpande do not provide any generalized equation to calculate the delay of a circuit, while the other method in uses fan out which is strongly prohibited in reversible logic design. On the other hand, the proposed circuit is designed avoiding the fan outs. The design also failed to preserve

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the constraint of reversible logic design, i.e., loop in circuit. The proposed reversible multiplier works without using feedback and also can operate on both positive and negative numbers whereas the existing reversible multiplier work as serial multiplier. This achievement is obtained in expense of delay and preserving reversibility.

5 CONCLUSION

This paper presents a Radix-2 Booth's Multiplier implementation using Reversible Gates. A full design of n × n reversible array multiplier is proposed which is based on the conventional irreversible design. The evaluation of the proposed circuit is performed from all the aspects of reversible logic. Additionally, the quantum cost of the proposed cell (different sub-sections of the entire circuit) as well as the whole design has been analyzed. The proposed reversible multiplier architecture outperforms the existing design in terms of design methodology by preserving the constraints of reversible logic synthesis. The key achievement of the design is, it is capable of working with both signed and unsigned numbers, which is not present in the existing circuits considered in this paper. Current research is investigating the extension of the proposed logic for Radix-4 approach.

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